500.28006C10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	M. HORIGUCHI et al
Serial No.:	(New Continuation application under 37 CFR §1.53[b] Of U.S. Application Serial No. 10/401,975)
Filed:	On Even Date Herewith
For:	A SEMICONDUCTOR DEVICE HAVING REDUNDANCY CIRCUIT
Group:	2824
Examiner:	J. HUR

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 & §1.98

MS: Patent Applications
Commissioner For Patents
POB 1450
Alexandria, VA 22313-1450

March 31, 2004

Sir:

In the matter of the above-identified application, applicants are attaching hereto, in a form equivalent to Form PTO-1449, a listing of all the art documents of record (cited by the Examiner/submitted by applicants) in the chain of continuing applications (as listed on page 1 of the Specification), pursuant to the duty of disclosure/candor requirements.

This Information Disclosure Statement is being submitted concurrently with the filing of the above-identified continuation application and, therefore, this IDS meets the requirements pursuant to 37 CFR §1.97(b).

As to the requirement of 37 CFR §1.98(a)(3) for any concise explanation of relevance to the extent that any of the listed documents is not in the English language, this is met by: the discussion thereof of JP 60-130139 (listing AM) in

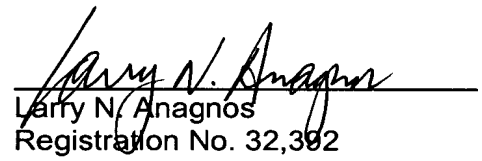
the background portion in the original Specification, the submission of an English language translation thereof of JP 62-40700 (listing AN), the submission thereof of USP 4,656,610 (which is an English language counterpart of JP 59-135700) and the citation by the Examiner in the prior application(s).

It is understood that since copies of the listed documents should be available in the file wrapper of the prior applications, copies thereof are not included herewith, consistent with 37 CFR §1.98(d) and pursuant to the guidelines set forth in MPEP §609.

It is submitted this IDS is in compliance with the rules of practice as well as with USPTO guidelines. Therefore, applicants respectfully request that it be entered and duly considered by the USPTO. Also, acknowledgment of entry as well as of formal consideration thereof by the Examiner is respectfully requested.

If any costs are due in accordance with the filing of this Information Disclosure Statement, please charge same to the account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (500.28006C10).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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Sheet 1 of 1

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		500.28006C10	R53(b) Cont. of S.N. 10/401,975
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT: M. HORIGUCHI, et al.	
		FILING DATE: March 31, 2004	GROUP: 2824

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	4,675,845	6/87	Itoh, et al.	365	51	
	AB	4,389,715	6/83	Eaton, Jr., et al.	365	200	
	AC	4,727,516	2/88	Yoshida, et al.	365	200	
	AD	4,648,075	3/87	Segawa, et al.	365	200	
	AE	4,837,747	6/89	Dosaka, et al.	365	200X	11/30/97
	AF	5,265,055	11/93	Horiguchi, et al.	365	200	10/10/89
	AG	5,617,365	4/97	Horiguchi, et al.	365	200	10/10/89
	AH	4,656,610	4/87	Yoshida, et al.	365	200	
	AI	5,815,448	9/98	Horiguchi, et al.	365	200	10/10/89
	AJ	4,752,914	06/88	Nakano et al	365	200	
	AK	6,577,544	06-03	Horiguchi et al	365	200	
	AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM	60-130139	11/85	Japan				
	AN	62-40700	2/87	Japan			X	
	AO	59-135700	8/84	Japan			**	
	AP			**see listing AH above				
	AQ							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 5, October 1981, pp. 479-487.
	AS	IEEE PROC., Vol. 130, Pt. I, No. 3, June 1983, pp. 127-135.
	AT	1984 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 282-283.
	AU	IEEE Journal of Solid-State Circuits, Vol. 26, No. 1, January 1991, pp. 12-17.
	AV	"System for Efficiently Using Spare Memory Components for Defect Corrections Employing Content-Addressable Memory," IBM Technical Disclosure Bulletin, vol. 28, no. 6, November 1985, pp. 2562-2567.

Examiner	Date Considered